Remarks

The above Amendments and these Remarks are in reply to the Office Action mailed September 10, 2004. A Petition for Extension of Time to Respond is submitted herewith, together with the appropriate fee.

I. Summary of Examiner's Rejections

Prior to the Office Action mailed September 10, 2004, Claims 1-24 were pending in the Application. In the Office Action mailed September 10, 2004, the Specification was objected to for various informalities. Claims 1, 2, 3, 6, 7, 10, 11, 21-23 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1, 3, 4, 6 and 7 of co-pending Application No. 09/560,844 in view of Mendel (U.S. Patent No. 6,080,204). Claims 1-15, 19-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (U.S. Patent No. 6,477,683, hereafter Killian) in view of Mendel. Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Rajsuman et al. (U.S. Patent No. 6,678,645, hereafter Rajsuman). Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of MicroSim ("MicroSim pSpice A/D & Basics + Circuit Analysis Software, User's Guide", Version 8.0, June 1997). Claim 24 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Kang et al. ("CMOS Digital Integrated Circuits, Analysis and Design", Second Edition, WCB/McGraw Hill, 1999, hereafter Kang).

II. Summary of Applicant's Amendment

The present Response amends the Specification; and also amends Claims 1 and 10; leaving for the Examiner's present consideration Claims 1-24. Reconsideration of the Application, as amended, is respectfully requested. Applicant reserves the right to prosecute any originally presented or canceled claims in a continuing or future application.

III. Amendments to the Specification

In the Office Action mailed September 10, 2004, the Specification was objected to for various informalities. Accordingly, the Specification has been amended, as shown in detail above to correct the informalities. Applicant respectfully submits that t no new matter is being added.

IV. Claim Rejections under Double Patenting

In the Office Action mailed September 10, 2004, Claims 1, 2, 3, 6, 7, 10, 11, 21-23 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1, 3, 4, 6 and 7 of co-pending Application No. 09/560,844 in view of Mendel (U.S. Patent No. 6,080,204). Accordingly, being filed together with this Response is a Terminal Disclaimer in compliance with 37 C.F.R. 1.321(c). Applicant respectfully submits that this renders moot the rejection of the Claims 1, 2, 3, 6, 7, 10, 11, 21-23 under the doctrine of double patenting, and reconsideration thereof is respectfully requested.

V. Claim Rejections under 35 U.S.C. § 103(a)

In the Office Action mailed September 10, 2004, Claims 1-15, 19-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (U.S. Patent No. 6,477,683, hereafter Killian) in view of Mendel (U.S. Patent No. 6,080,204).

Claim 1

Claim 1 has been amended to more clearly define the embodiment therein. As amended, Claim 1 currently defines:

1. (Currently Amended) A method of simultaneously optimizing performance characteristics in circuit synthesis, comprising the steps of:

(a) generating a set of circuit parameters for each performance characteristic of a circuit;

(b) simultaneously passing each said set of circuit parameters through a respective circuit model, wherein additional sets of circuit parameters may be passed at the same time in parallel;

(c) running a simulation of each said circuit model on an analysis test bench in order to measure performance of said circuit model using said set of circuit parameters, each said analysis test bench adapted to model circuitry external to said circuit and control the type of analysis to be performed for each said performance characteristic of said circuit; and

(d) receiving the performance measurements for each simulation at an optimizer and determining for which performance characteristics the specifications are met, and, for those analyses where the specifications are not met then generating new parameter values and repeating steps (a) through (d).

As amended, Claim 1 defines that the method comprises a step of simultaneously passing each of said set of circuit parameters through a respective circuit model, wherein additional sets of circuit parameters may be passed at the same time in parallel. Claim 1 further defines a step of receiving the performance measurements for each simulation at an optimizer and determining for which performance characteristics the specifications are met, and, for those analyses where the specifications are not met then generating new parameter values and repeating steps (a) through (d). Applicant respectfully submits that these features are neither disclosed nor suggested by the cited references.

In particular, Applicant respectfully submits that the claimed invention appears to be directed to a different goal from that of the cited references. In a traditional system for circuit design, since multiple models and test benches are required to measure all of the performance specifications, the optimization of each specification is usually a serial process. For example, a first type of analysis is usually performed using a set of circuit parameters, a circuit model, and a test bench for a first simulation. Performance is then measured for that analysis. A second type of analysis is usually performed using another set of circuit parameters, another circuit model, and another test bench for a second simulation. Since this is a serial process, each individual simulation must be

completed before the next simulation in that set can begin. Every additional analysis adds directly to the time required to complete one set of evaluations.

However, in accordance with an embodiment of the present invention, for each additional specification that is added, the additional simulation is performed concurrently with all other simulations. From a starting set of parameter values, a set of circuit parameters is generated for each specification. Each set of circuit parameters is then passed simultaneously through the appropriate circuit models, analysis test benches, simulations, and performance measurements, as if each simulation was done separately. The optimizer receives the performance measurements for each simulation and determines whether the specifications were met. For those analyses where the specifications are not met then the process is repeated, generating new parameter values, and again passing those new circuit parameters simultaneously through the appropriate circuit models, analysis test benches, simulations, and performance measurements.

Killian discloses an automated processor generation system for designing a configurable processor and method for the same. Killian teaches providing an automated processor generation system which uses a description of customized processor instruction set options and extensions in a standardized language to develop a configured definition of a target instruction set, a Hardware Description Language description of circuitry necessary to implement the instruction set, and development tools such as a compiler, assembler, debugger and simulator which can be used to generate software for the processor and to verify the processor. Implementation of the processor circuitry can be optimized for various criteria such as area, power consumption and speed. Once a processor configuration is developed, it can be tested and inputs to the system modified to iteratively optimize the processor implementation.

However, Applicant respectfully submits that Killian does not appear to teach that any of these steps can be performed simultaneously. Indeed, Killian appears to follow the traditional process of performing each of its steps in a serial fashion.

Mendel discloses a method and apparatus for contemporaneously compiling an electronic circuit design by contemporaneously bipartitioning the electronic circuit design using parallel processing. Mendel teaches that disclosed methods identify "compilation tasks" that can be

performed in isolation from the remainder of a large "compilation project." When one of these stand alone compilation tasks is identified, it can be temporarily segregated and performed by one or more processors which are not working on other tasks. Simultaneously, the remainder of the project compiles under one or more other processors.

However, Applicant respectfully submits that Mendel appears to require that the compilation tasks be separable, in order for them to be segregated and performed by separate processors. In this manner, Mendel differs from the present invention in that the tasks performed herein are not amenable to being segregated. Instead, the process defined by Claim 1 includes generating a set of circuit parameters for each performance characteristic of a circuit; and simultaneously passing each said set of circuit parameters through a respective circuit model, wherein additional sets of circuit parameters may be passed at the same time in parallel. As described in Applicant's Specification, additional processors or CPU's could be used to perform the process for multiple circuit models at the same time, but this is an aspect of other embodiments of the invention. The simultaneously passing of each said set of circuit parameters through a respective circuit model is not itself segregated, since to do so would defeat the purpose of running a simulation of each said circuit model on an analysis test bench in order to measure performance of said circuit model using said set of circuit parameters, each said analysis test bench adapted to model circuitry external to said circuit and control the type of analysis to be performed for each said performance characteristic of said circuit.

In view of the above comments, Applicant respectfully submits that Claim 1 is neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested.

Claim 10

The comments provided above with respect to Claim 1 are incorporated herein by reference. Claim 10 has been similarly amended to more clearly define the embodiment therein as including a step of simultaneously passing each of said set of circuit parameters through a respective circuit model, wherein additional sets of circuit parameters may be passed at the same time in parallel.

Claim 10 further defines comprising an optimizer that determines for which performance characteristics the specifications are met, and, for those analyses where the specifications are not met then generating new parameter values and repeating the simulation with the new parameter values. In view of the above-described amendments to Claim 10, and for similar reasons as given above with respect to Claim 1, Applicant respectfully submits that Claim 10 is similarly neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested.

Claims 2-9, 11-15 and 19-23

Claims 2-9, 11-15 and 19-23 are not addressed separately but it is respectfully submitted that these claims are allowable as depending from an allowable independent claim and further in view of the comments provided above. Applicant respectfully submits that Claims 2-9, 11-15 and 19-23 are similarly neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested. It is also submitted that these claims also add their own limitations which render them patentable in their own right. Applicant reserves the right to argue these limitations should it become necessary in the future.

Claims 16 and 17

In the Office Action mailed September 10, 2004, Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Rajsuman et al. (U.S. Patent No. 6,678,645, hereafter Rajsuman). Claims 16 and 17 are not addressed separately but it is respectfully submitted that these claims are allowable as depending from an allowable independent claim and further in view of the comments provided above. Applicant respectfully submits that Claims 16 and 17 are similarly neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested. It is also submitted that these claims also add their own limitations which render them patentable in their own right. Applicant reserves the right to argue these limitations should it become necessary in the future.

Claim 18

In the Office Action mailed September 10, 2004, Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of MicroSim ("MicroSim pSpice A/D & Basics + Circuit Analysis Software, User's Guide", Version 8.0, June 1997). Claim 18 is not addressed separately but it is respectfully submitted that the claim is allowable as depending from an allowable independent claim and further in view of the comments provided above. Applicant respectfully submits that Claim 18 is similarly neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested. It is also submitted that the claim also adds its own limitations which renders it patentable in its own right. Applicant reserves the right to argue these limitations should it become necessary in the future.

Claim 24

In the Office Action mailed September 10, 2004, Claim 24 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Kang et al. ("CMOS Digital Integrated Circuits, Analysis and Design", Second Edition, WCB/McGraw Hill, 1999, hereafter Kang). Claim 24 is not addressed separately but it is respectfully submitted that the claim is allowable as depending from an allowable independent claim and further in view of the comments provided above. Applicant respectfully submits that Claim 24 is similarly neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested. It is also submitted that the claim also adds its own limitations which renders it patentable in its own right. Applicant reserves the right to argue these limitations should it become necessary in the future.

VI. Conclusion

In view of the above amendments and remarks, it is respectfully submitted that all of the claims now pending in the subject patent application should be allowable, and reconsideration thereof is respectfully requested. The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, March 10, 2005.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: March 10, 2005 By: _____

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